The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Fall 2010
Sample Test 3

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

1. (1 point) Storage elements that operate with signal levels (rather than signal transitions) are referred to as _____

2. (1 point) A _____ defines the logical properties of a flip-flop by describing its operation in tabular form.

3. (1 point) Some flip-flops have _____ inputs that are used to force the flip-flop to a particular state independent of the clock.

4. (1 point) The time sequence of inputs, outputs, and flip-flop states can be enumerated in a _____.

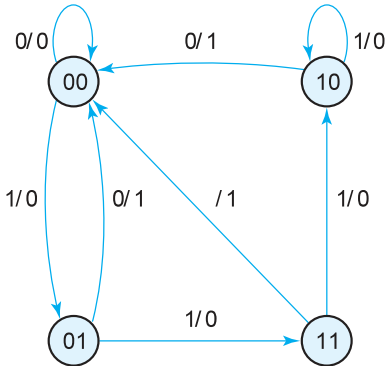
5. (1 point) In Verilog, behavior declared by the keyword **initial** is called _____ behavior.

6. (20 points) An .LM flip-flop has four operations, set to 1, no change, complement, and clear to 0, when inputs are P and N are 00, 01, 10, and 11, respectively.
   (a) Tabulate the characteristic table.
   (b) Derive the characteristic equation.
   (c) Tabulate the excitation table.

7. (15 points) Reduce the number of states in the following state table, and tabulate the reduced state table:

	Next State		Present Output (Z)
Present State	x = 0	x = 1	
a	b	a	0
b	c	a	0
c	d	g	0
d	a	e	0
e	f	a	0
f	a	a	1
g	h	a	0
h	i	a	0
i	a	a	1

8. (15 points) Starting from state 00 in the state diagram shown, determine the state transitions and output sequence that will be generated when an input sequence of 10110001110100111101010 1 is applied



Current State	Input	Next State	Output

9. (25 points) Design a 3-bit counter which counts in the sequence 001, 011, 010, 110, 101, 100, 001 using clocked D flip-flops. What will happen if the counter is started in state 000?

10. (20 points) Design a sequential circuit that behaves in the following way. When a sequence of 0's and 1's is applied to the X input, the output of the network is Z =1 If the total number of 1 inputs received is odd. Otherwise the output is Z = 0. (0 is an even number). Use JK flip-flops. You do not have to draw the circuit diagram.