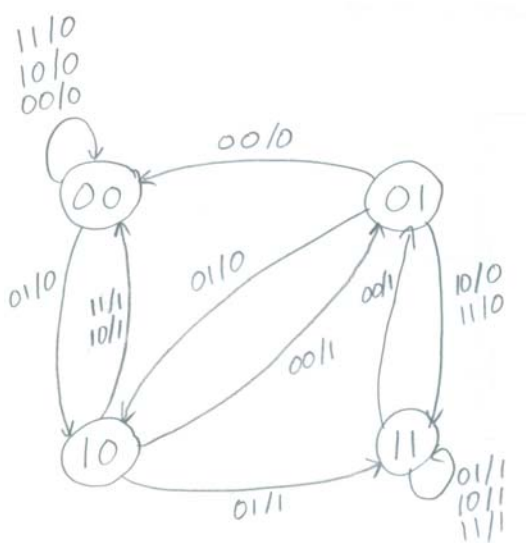
The University of Alabama in Huntsville
ECE Department
EE 202 – 02
Fall 2010
Test 3 Solution

J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	Q'(t)

D	Q(t+1)
0	0
1	1

T	Q(t+1)
0	Q(t)
1	Q'(t)

1. (1 point) Storage elements that operate with signal levels (rather than signal transitions) are referred to as _latches_
2. (1 point) A _characteristic table_ defines the logical properties of a flip-flop by describing its operation in tabular form.
3. (1 point) Some flip-flops have _aynchronous_ inputs that are used to force the flip-flop to a particular state independent of the clock.
4. (1 point) The time sequence of inputs, outputs, and flip-flop states can be enumerated in a _state table_.
5. (1 point) In Verilog, behavior declared by the keyword **initial** is called _first-pass_ behavior.
6. (15 points) Starting from state 00 in the state diagram shown, determine the state transitions and output sequence that will be generated when an input sequence of 00, 11, 10, 01, 11, 10, 01, 00, 10, 10, 00, 01, 01, 11, 11, 00, 00



Current State	Input	Next State	Output
00	00	00	0
00	11	00	0
00	10	00	0
00	01	10	0
10	11	00	1
00	10	00	0
00	01	10	0
10	00	01	1
01	10	11	0
11	10	11	1
11	00	01	1
01	01	10	0
10	01	11	1
11	11	11	1
11	11	11	1
11	00	01	1
01	00	00	0

7. (20 points) A .UAH flip-flop has four operations, clear to 0, set to 1, no change, and complement, when inputs are P and N are 00, 01, 10, and 11, respectively.

(a) Tabulate the characteristic table.

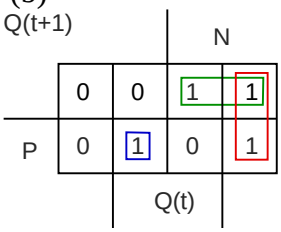
(b) Derive the characteristic equation.

(c) Tabulate the excitation table.

(a)

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

(b)



Q(t+1) = P'N + NQ' + PN'Q

(c)

Q(t)	Q(t+1)	P	N
0	0	d	0
0	1	d	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

8. (15 points) Reduce the number of states in the following state table, and tabulate the reduced state table:

	Next State		Output	
Present State	x = 0	x = 1	x = 0	x = 1
S0	S1	S4	0	0
S1	S2	S1	0	0
S2	S1	S6	0	0
S3	S1	S3	0	0
S4	S5	S4	0	0
S5	S2	S1	0	0
S6	S5	S3	0	1

S5 = S1

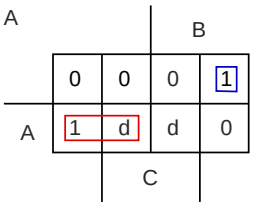
	Next State		Output	
Present State	x = 0	x = 1	x = 0	x = 1
S0	S1	S4	0	0
S1	S2	S1	0	0
S2	S1	S6	0	0
S3	S1	S3	0	0
S4	S1	S4	0	0
S6	S1	S3	0	1

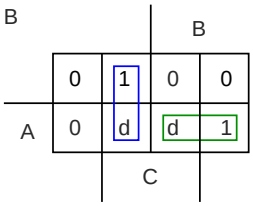
S4 = S0

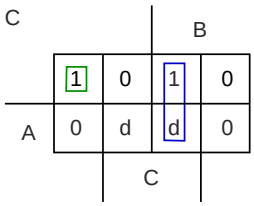
	Next State		Output	
Present State	x = 0	x = 1	x = 0	x = 1
S0	S1	S0	0	0
S1	S2	S1	0	0
S2	S1	S6	0	0
S3	S1	S3	0	0
S6	S1	S3	0	1

9. (25 points) Design a 3-bit counter which counts in the sequence 001, 011, 010, 110, 100, 000, 001 using clocked T flip-flops. You do not have to draw the circuit diagram. What will happen if the counter is started in state 111?

Present State, ABC	Next State, ABC	Flip-Flop Inputs, $T_AT_BT_C$
001	011	010
011	010	001
010	110	100
110	100	010
100	000	100
000	001	001





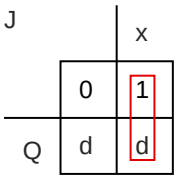


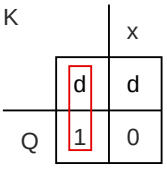
A = AB' + A'BC' B = AB + B'C C = BC + A'B'C'

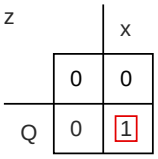
10. (20 points) Design a Mealy sequential circuit that has an output of 1 whenever its input string has at least two 1s in sequence and otherwise has an output of 0. Use JK flip-flops. You do not have to draw the circuit diagram.

Input: 00101011101000111110101010111000011001
Output: 00000001100000011110000000011000001000

	Next State		Output		J		K	
Present State	x = 0	x = 1	x = 0	x = 1	x = 0	x = 1	x = 0	x = 1
0	0	1	0	0	0	1	d	d
1	0	1	0	1	d	d	1	0







J = x K = x' z = xQ